TITLE **800G QSFP-DD PAM4 Active Copper Cable**	**DOC No. RFD-20240226012-002**	
	REVISION：01	**AUTHORIZED BY：Albert Lin**
	DATE：2024/02/27	**CLASSIFICATION：Active Copper Cable**

1. DESCRIPTION

QSFP-DD active copper cable assembly feature sixteen differential copper pairs, providing eight data transmission channels at speeds up to 100Gbps (PAM4) per channel, and meets 800G Ethernet and InfiniBand Next Data Rate (NDR) requirements. Available in a broad range of wire gages from 26AWG through 30AWG-this 800G copper cable assembly features low insertion loss and low crosstalk.

QSFP-DD uses PAM4 signals for transmission, which doubles the rate. However, there are more stringent requirements for cable insertion loss. For detailed requirements, please see High Speed Characteristics.

2. PRODUCT FEATURES

- Compatible with IEEE 802.3ck
- Supports aggregate data rates of 800Gbps (PAM4)
- Optimized construction to minimize insertion loss and cross talk.
- Pull-to-release slide latch design.
- Straight and break out assembly configurations available.
- Customized cable braid termination limits EMI radiation
- Customizable EEPROM mapping for cable signature
- 26AWG through 30AWG cable
- 3.3V Power supply
- Low power Consumes 0.15W per active channel, the total power of the cable is 2.5W
- EQ programmable
- Temperature Range: 0~ 70 °C

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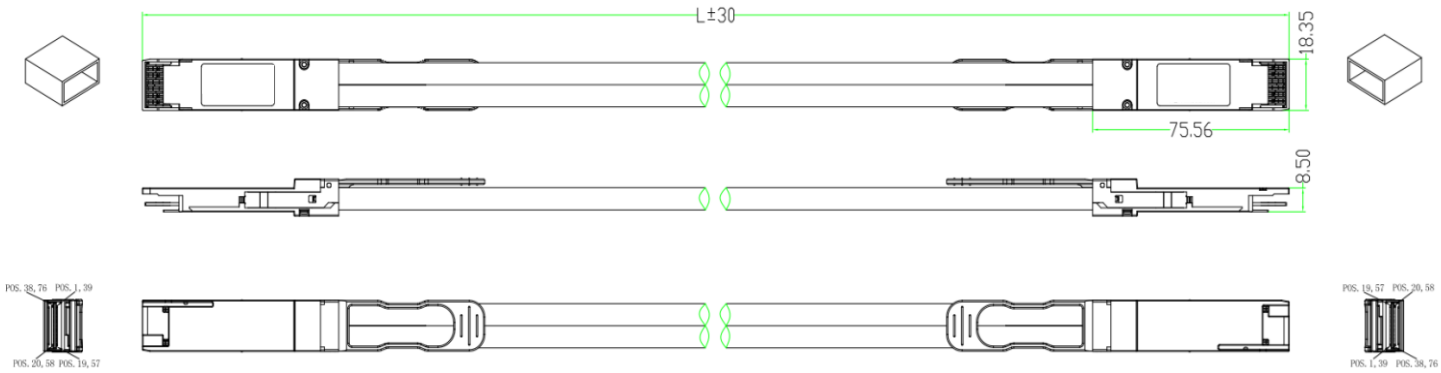
3. PRODUCT DESCRIPTION

3.1 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



Length (m)	Cable AWG
1	30
2	30
3	30
4	26
5	26

4. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- Switches, servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment.

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- 800G Ethernet (IEEE 802.3ck)
- InfiniBand NDR

5. Absolute Maximum Ratings & Recommended Operating Conditions

General Product Characteristics	
Parameter	
Number of Lanes	Tx8 & Rx8
Channel Data Rate	106.25Gbps
Operating Temperature	0 to + 70°C
Storage Temperature	-40 to + 85°C
Supply Voltage	3.3 V nominal
Electrical Interface	76pins edge connector
Management Interface	Serial, I^2C

High Speed Characteristics						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Note**
Differential Impedance	TDR	90	100	110	Ω	
Insertion loss	SDD21	-19.75			dB	4
Differential Return Loss	SDD11 SDD22			See 1	dB	5
				See 2	dB	6
Common-mode to common-mode output return loss	SCC11 SCC22			-2	dB	7
Differential to common Mode Conversion Loss	SCD21- SDD21			-10	dB	8
				See3	dB	9

Notes:
1. Reflection Coefficient given by equation SDD11(dB) <22-10(f/26.56), with f in GHz.
2. Reflection Coefficient given by equation SDD11(dB) <15-3(f/26.5), with f in GHz.
*3. Reflection Coefficient given by equation SCD21-CDD21(dB) < 14-0.3108*f, with f in GHz.*

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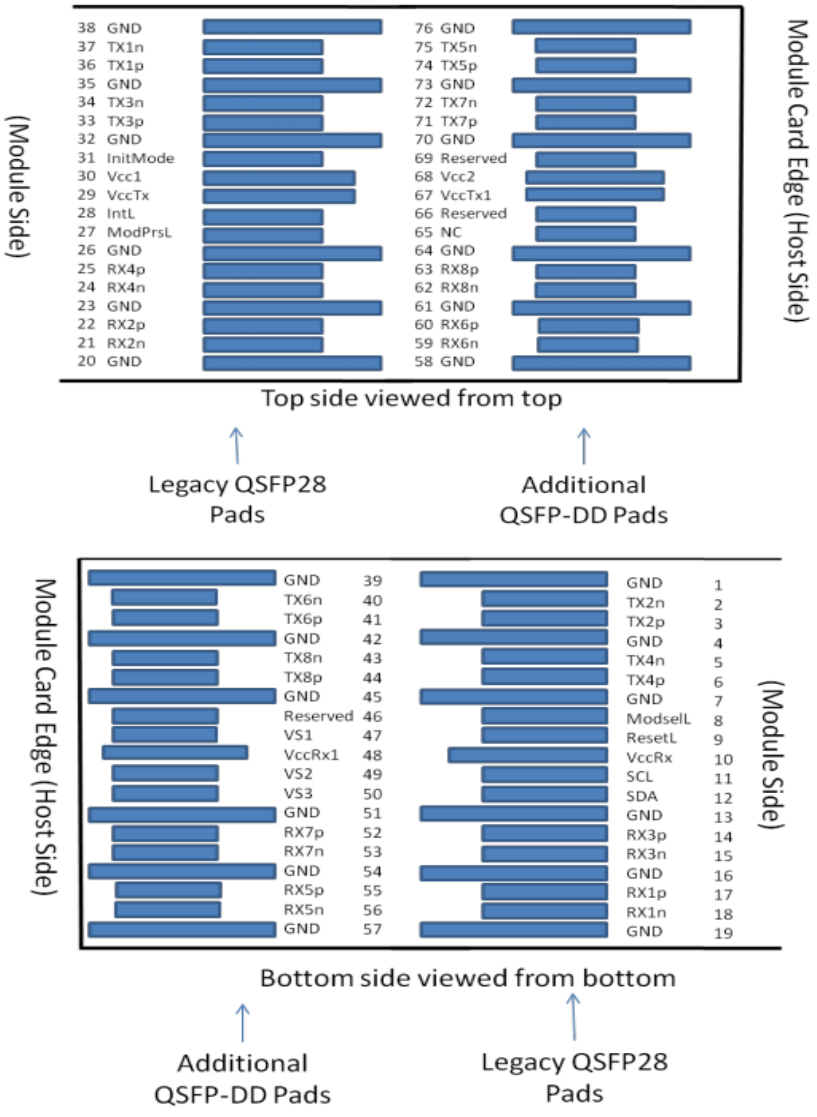
4. At 26.56 GHz.
5. At 0.05 to 26.56 GHz.
6. At 26.56 to 40 GHz.
7. At 0.2 to 40 GHz.
8. At 0.05 to 12.89 GHz.
9. At 12.89 to 40 GHz.

6. Pin-out Definition:



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Pin Definitions

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVCMOS- I/O	SCL	2-wire serial interface clock
12	LVCMOS- I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output

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25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		Vcc Tx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	LPMode	Low Power Mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46		Reserved	
47		VS1	
48		VccRx1	+3.3V Power supply
49		VS2	
50		VS3	

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51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	
66		Reserved	
67		VccTx1	+3.3V Power supply
68		VCC2	+3.3V Power supply
69		Reserved	
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

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7. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2024/02/27	Albert Lin	Mike Sun